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UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>	Attorney Docket No	97RSS 256-DIV	Total Pages	7
	First Named Inventor or Application Identifier			
	Zhao et al.			
Express Mail Label No		EJ391163432 US		

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
1. <input checked="" type="checkbox"/> Fee Transmittal Form <small>(Submit an original, and a duplicate for fee processing)</small> 2. <input checked="" type="checkbox"/> Specification [Total Pages 21] - Descriptive title of the invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the invention - Brief Summary of the invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure 3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) [Total Sheets 15] 4. Oath or Declaration [Total Pages 2] a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <small>(for continuation/divisional with Box 17 completed)</small> <small>(Note Box 5 below)</small> i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 5. <input type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.	6. <input type="checkbox"/> Microfiche Computer Program (Appendix) 7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies
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17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:
☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: 09, 158,337

18. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label or ☒ Correspondence address below
(Insert Customer No. or Attach bar code label here)

NAME	Philip K. Yu				
	Rockwell Semiconductor Systems				
ADDRESS	c/o Intellectual Property Dept., Mail Code E09-900				
	4311 Jamboree Road				
CITY	Newport Beach	STATE	CAL.	ZIP CODE	92660
COUNTRY	USA	TELEPHONE	949-483-3203	FAX	949-483-3206

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application Serial No: 09/158,337

Prior Examiner: Edwin Oh

Prior Art Unit: 2822

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REQUEST FOR FILING OF DIVISIONAL
APPLICATION UNDER 37 CFR 1.53(b)

This is a request for filing a:

[] continuation application

[X] divisional application

pursuant to 37 CFR 1.53(b), of pending prior application Serial No. 09/158,337, filed on September 22, 1998, of Zhao et al. for "Interconnect With Low Dielectric Constant Insulators For Semiconductor Integrated Circuit Manufacturing".

1. [X] Enclosed is a copy of the prior application, including the oath or declaration as originally filed.

I hereby verify that the attached papers are a true copy of the prior application Serial No. 09/158,337, as originally filed on September 22, 1998, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. [X] Amend the specification by inserting before the first line the following sentence:

-- 1. Related Cases

This is a division of co-pending Serial No. 09/158,337, entitled "Interconnect With Low Dielectric Constant Insulators For Semiconductor Integrated Circuit Manufacturing", filed September 22, 1998, the entire disclosure of which is incorporated by this reference as though set forth fully herein.--

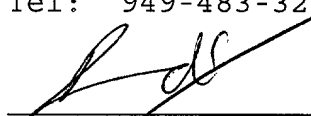
3. [X] A check in the amount of \$760.00 for the filing fee is enclosed. This fee is calculated as follows:

	Claims Remaining After Amendment	Number Extra	Rate	Fee	Large Entity	Rate	Fee	Small Entity
Basic Fee				\$760			\$380	
Total Claims	12 - 20 = 0	x	\$18 =		x	\$9 =	0	
Indep. Claims	1 - 3 = 0	x	\$78 =		x	\$39 =	0	
Multiple Dependent Claims	+		\$260 =		+	\$130 =		
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4. [X] Cancel in this application original claims 1-15 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)
5. [X] The power of attorney appears in the original papers in prior application Serial No. 09/158,337, filed on September 22, 1998.
6. [X] Address all future communications to:

Philip K. Yu, Reg. No. 35,742
 Conexant Systems Inc. (formerly Rockwell Semiconductor Corp.)
 4311 Jamboree Road, E09-900
 Newport Beach, California 92660-3095
 Tel: 949-483-3203

By:


 RAYMOND SUN
 Reg. No. 35,699
 Attorney for Applicant
 Conexant Systems Inc. (formerly Rockwell Semiconductor Corp.)
 4311 Jamboree Road, E09-900
 Newport Beach, California 92660-3095
 Tel: 949-483-3203

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UNITED STATES PATENT APPLICATION FOR
INTERCONNECT WITH LOW DIELECTRIC CONSTANT
INSULATORS FOR SEMICONDUCTOR INTEGRATED
CIRCUIT MANUFACTURING

Inventors:
Bin Zhao
Maureen Brongo

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to semiconductor processing, and more specifically to multi-level interconnects with low dielectric constant insulators and methods for
5 fabricating the same.

2. Background Art

Modern integrated circuits are made up of literally millions of active and passive devices such as transistors, capacitors, and resistors. These devices are initially isolated from one another but are later connected together to form functional circuits through
10 interconnect structures. The quality of the interconnect structure drastically affects the performance and reliability of the fabricated circuit. Interconnects are increasingly determining the limits of performance and density of modern ultra large scale integrated (ULSI) circuits.

Conventional interconnect structures employ one or more metal layers. Each
15 metal layer is typically made from aluminum alloys or tungsten. Interlevel and intralevel dielectrics (ILDs), such as silicon dioxide (SiO_2), are used to electrically isolate active elements and different interconnect signal paths from each other. The electrical connections between different interconnect levels are made through vias that are formed in the ILD layers. Typically, the vias are filled with a metal, such as tungsten.

20 Recently, there has been great interest to replace SiO_2 with low-dielectric-constant ("low-k") materials as the ILD in interconnect structures. It is desirable to employ low-k materials as insulators in IC interconnect because these low-k materials reduce the interconnect capacitance. Accordingly, these low-k materials increase the signal propagation speed while reducing cross-talk noise and power dissipation in the
25 interconnect.

However, the use of low-k materials as ILD in the interconnect is not mature at this time, and processes still need to be developed for accommodating the low-k material when forming the interconnect. When forming ILDs entirely out of low-k materials, almost all interconnect processing steps need to be developed, such as the following steps:
30 chemical mechanical polishing (CMP) of the low-k materials, via etch into the low-k ILD layer, post via etch clean, and metal via fill into the low-k ILD layer.

Attempts have been made to provide a process for an embedded low-k dielectric integration approach that employs the low-k dielectric for filling only the gaps between metal lines in the interconnect structure, while still employing conventional SiO₂ in the rest of the ILD. U.S. Patent No. 5,486,493 to Jeng, entitled "Planarized Multi-level
5 Interconnect Scheme With Embedded Low-Dielectric Constant Insulators," describes one such approach to embed low-k dielectric in the interconnect structure.

The advantage of this approach is that, since the low-k film is only used to fill the gaps between the metal lines, many of the above-mentioned interconnect processing steps are the steps utilized for conventional SiO₂ ILD. This approach attempts to avoid
10 the difficulties associated with (1) having to etch a via through a low-k film; (2) having to make the post-via-etch clean for the low-k film, and (3) having to fill metal through the low-k film for the via plugs.

Unfortunately, these embedded low-k dielectric integration processes suffer from the following disadvantages. For example, ensuring that the level of the low-k material is
15 the same as the top surfaces of the metal or interconnect lines is difficult for at least four reasons. First, in practical manufacturing, it is impossible to deposit a film of low-k material at a precise film thickness from wafer to wafer. Second, even within a wafer, depositing an absolutely uniform low-k film across the same wafer is not possible, since the typical thickness non-uniformity of the low-k film deposited by either spin-on coating or
20 chemical vapor deposition (CVD) using currently-available technology varies by about one to ten percent. Third, even within a given die on a wafer, the gaps between the metal lines are of different sizes, leading to uneven film height of the low-k material above the metal lines. The larger gaps or spacings are filled with more low-k material, thereby lowering the height of the low-k material in these areas. In contrast, the smaller gaps or
25 spacing are filled with less low-k material, thereby raising the height of the low-k material in these areas. Fourth, removing low-k film to the precise thickness during the etch-back is impossible to control in manufacturing.

This difficulty of controlling the deposition and etch-back of the low-k material so that the surface level of the low-k material is the same as the top surfaces of all the metal

or interconnect lines results in the following two problems: (1) insufficient-etch-back of the low-k material, which results in a poisoned via and problems associated therewith, and (2) excessive-etch-back of the low-k material, which results in the increase in inter-metal line capacitance and problems associated therewith.

5 Consequently, applying the correct etch-back amount for the low-k material with the required tolerance (hereinafter referred to as a "process window") is difficult for these proposed processes that embed low-k materials. This problem can be characterized as: "the low-k material etch-back has a very narrow process window." Missing the process window, for whatever reason, results in poor interconnect integrity and reliability, or
10 degradation in interconnect performance.

15 A conventional method for embedding a low dielectric constant (low-k) material in an interconnect structure involves the following process steps. A first metal layer is deposited on a substrate 1 and patterned to form metal lines 2. Thereafter, a low-k dielectric material 3 is deposited over substrate 1 and metal lines 2. FIG. 1A illustrates a cross-section view of a conventional interconnect structure after the step of depositing the low-k material 3 over substrate 1 and metal lines 2. An etch-back is used to etch the low-k material 3 such that the low-k dielectric material 3 only fills the gaps between metal lines 2 as shown in FIG. 1B. An SiO₂ layer 4 is then deposited and planarized. Via holes 5 are etched in the SiO₂ layer 4. Metal plugs 6 are formed in the via holes 5. Thereafter, a
20 second metal layer is deposited on the SiO₂ layer 4 and patterned to form metal lines 7. FIG. 1B illustrates a cross sectional view of an ideal conventional embedded low-k interconnect structure after the step of depositing and patterning the second metal layer.

25 In the ideal case, the low-k dielectric material 3 is isolated from the chemicals utilized to etch and clean the via holes 5 and the chemicals utilized to deposit the metal plugs 6. However, as explained above, the etch-back of the low-k material 3, which is critical for this isolation to occur, is difficult to control. Consequently, instead of the ideal case where the low-k material 3 is etched-back exactly at the top level of the metal or interconnect, the more likely case is that either the low-k material 3 is insufficiently etched-back or excessively etched-back.

FIG. 1C illustrates a cross section of a conventional interconnect structure in which the etch-back of the low-k material is insufficient (i.e., the height or level of the low-k dielectric material 3 is higher than the height of the metal lines 2). When the etch-back of the low-k material 3 is insufficient, poisoned vias 8 result. A poisoned via 8 is caused by the exposure of the low-k material 3 to the chemicals that are used in the subsequent via etch, photoresist strip and wet clean processing steps and that are not compatible with the low-k material 3. The poisoned vias 8 present a serious yield and reliability problem in the conventional embedded low-k interconnect structures. The poisoned vias 8 lead to high via or contact or even via failure. Specifically, the bowl shape of poisoned vias 8 prevents the formation of a continuous seed layer or liner that is a precursor to filling the vias with plug metals. A discontinuous liner leads to poor metal growth and a poor connection.

FIG. 1D illustrates a cross section of a conventional interconnect structure in which the etch-back of the low-k material 3 is excessive (i.e., the low-k material is over-etched, exposing the sides 9 of the metal line to oxide). When the etch-back of the low-k material 3 is excessive, the capacitance between metal lines 2 (i.e., the inter-line capacitance) increases. A higher inter-line capacitance causes signals to propagate slower through the interconnect. Furthermore, the higher inter-line capacitance increases cross-talk noise, which is the unwanted transfer of signals from one metal line to another metal line.

Even if the process window is met for some metal lines, other metal lines may miss the process window. For example, the metal lines that are spaced further apart from each other experience excessive-etch-back of the low-k material (i.e., the level of the low-k material in these gaps are lower than the height of the metal lines) because the increased spacings between these metal lines. After the low-k dielectric etch-back, these spacings are only partially filled by the low-k material.

In summary, missing the process window leads to either poor interconnect integrity and reliability or degradation in performance of the circuits. Furthermore, it is very difficult or impossible to embed the low-k materials precisely in the metal gaps of different sizes by the low-k film deposition and the etch-back process. Consequently, the improvement

to the overall integrated circuit performance that is provided by the incorporation of low-k material is limited.

FIGS. 2A and 2B illustrate how misalignment of vias 5a (also known as "unlanded vias") can also cause poisoned vias. Even when the process window for the etch-back of the low-k material 3a is met, the misalignment of the vias 5a with respect to the underlying metal lines 2a can also cause poisoned vias 8a. Accordingly, it is important in conventional embedded low-k interconnect structures that the vias 5a be properly aligned (also known as "landed vias") to the underlying metal lines 2a in order to isolate the low-k material 3a from the metal plugs 6a. FIGS. 2A and 2B are cross sectional views that illustrate how vias 5a can be poisoned because of misalignment even when the process window for the etch-back of the low-k material 3a is met. As noted earlier, poisoned vias 8a lead to poor plug formation that results in poor contact between the metal layers.

To address this potential misalignment problem, attempts have been made to provide some misalignment tolerance during the manufacturing process. One such approach to achieve the isolation between via plugs 6a from the low-k material 3a is to provide a larger metal area 2a at the vias 5a, thereby providing the needed misalignment tolerance.

However, increasing the metal area causes several disadvantages. First, an increased metal area causes an increased pitch, thereby reducing interconnect density per layer. Since each wafer has a predetermined number of required interconnects, a reduced interconnect density per layer forces a designer to add additional layers of interconnects to meet the required number of interconnects. Adding additional layers of interconnects increases the costs to manufacture the wafer and can also lead to lower yields.

Second, even after the metal area has been increased, special care is still required to ensure that the wafers are processed within the misalignment tolerance provided by the increased metal area. Furthermore, the precautions of increased metal area and special care in processing do not preclude the possibility of a poisoned via resulting from misalignment of the via to the metal.

Accordingly, there remains a need for an interconnect structure and fabrication method that addresses the poisoned via problem that results from misalignment and the disadvantages set forth above.

5

SUMMARY OF THE INVENTION

An object of the present invention is to provide an interconnect structure and related fabrication process for addressing mis-aligned vias by employing a protective layer.

Another object of the present invention is to provide an interconnect structure and
10 related fabrication process that increases the process window for low-k etch-back by using a sacrificial layer.

The objects of the present invention may be accomplished by an improved interconnect that is formed on a semiconductor body and a corresponding fabrication method. A first metal layer is deposited on the semiconductor body. A sacrificial layer
15 having a height is deposited on the first metal layer. Thereafter, the first metal layer and the sacrificial layer are patterned to form metal lines having a sacrificial layer cap that are spaced apart from each other to form gaps therebetween. A low-k material is deposited as an embedded intra-level dielectric (ILD). The height of the sacrificial layer defines, and actually increases, the process window for the etch-back of the low-k material. After the
20 low-k material has been deposited, the low-k material is removed or etched back to a level which is at or within the height of the sacrificial layer. Planarization of the low-k material by CMP processing can also ensure that the process window is not missed. Thereafter, the sacrificial layer is removed, and a protective layer is deposited on the low-k material and the metal lines. A conventional dielectric layer, such as SiO₂, is then
25 deposited on the protective layer, and vias are etched therein. A photo-resist (PR) strip and via etch clean are then performed while the protective layer protects the low-k material from attack by chemicals utilized in these process steps. Thereafter, the protective layer is selectively etched so that the via plugs can contact the metal lines. The protective layer helps to shield the via metal from the low-k material.

Other objects and advantages of the present invention will become evident from the detailed description which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

5 The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

FIGS. 1A -1D illustrate conventional interconnect structures that embed low dielectric constant (low-k) material and the associated problems stemming from under-
10 etch and over-etch of the low-k material.

FIGS. 2A and 2B illustrate how vias can be poisoned because of misalignment of vias with the metal lines.

FIGS. 3A-3M are vertical cross sectional views that illustrate selected stages of fabrication of the interconnect structure according to a first embodiment of the present
15 invention for mis-aligned vias.

FIGS. 4A-4E are vertical cross sectional views that illustrate selected stages of fabrication of the interconnect structure according to the first embodiment of the present invention for perfectly aligned vias.

FIGS. 5A-5I are vertical cross-sectional views that illustrate selected stages of
20 fabrication of the interconnect structure according to a second alternative embodiment of the present invention.

FIGS. 6A-6D are vertical cross-sectional views that illustrate selected stages of fabrication of the interconnect structure according to a third alternative embodiment of the present invention.

25 FIG. 7A is a cross-sectional view of a via without a spacer after the step of depositing a barrier/seed layer.

FIG. 7B is a cross-sectional view of a via having a spacer after the step of depositing a barrier/seed layer.

DETAILED DESCRIPTION OF THE INVENTION

Multi-level interconnects with low dielectric constant insulators and methods for fabricating the same are disclosed herein. In the following detailed specification, numerous specific details are set forth, such as materials, thicknesses, processing
5 sequences, etc., in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without some of these specific details. In certain instances, well-known processing steps, device structures, semiconductor manufacturing materials, and equipment have not been described in detail in order to avoid unnecessarily obscuring the
10 present invention.

The present invention is now described in connection with the following three specific embodiments: (1) process utilizing a low-k etch-back step for mis-aligned vias and for perfectly aligned vias; (2) process utilizing a low-k polishing step; and (3) process
5 utilizing both a low-k polishing step and a low-k etch-back step.

FIRST EMBODIMENT: PROCESS UTILIZING A LOW-K ETCH-BACK STEP (MIS-ALIGNED VIAS)

FIGS. 3A-3M are vertical cross sectional views, illustrating selected stages of fabrication of the interconnect structure according to a first embodiment of the present
20 invention. Referring to FIG. 3A, a first metal layer 10x is deposited on a substrate 14x. First metal layer 10x can be any conductive material, such as polysilicon, TiN, Ti, Al, Al-alloy, TaN, Cu, Ta, or the combination of the above. The substrate 14x can contain silicon devices and previously-formed interconnect structures. A sacrificial layer (SL) 18x
25 is deposited on the first metal layer 10x according to methods known in the art. The sacrificial layer (SL) 18x can be an insulating or conductive material that is chemically different from metal layer 10x and a low-k material 26x that is later deposited (as described below), and can include but is not limited to silicon dioxide (SiO₂), silicon nitride (SiN), aluminum oxide (Al₂O₃), silicon carbide (SiC), polymers, or other organic materials. Sacrificial layer (SL) 18x can include a conductive material such as titanium, titanium

nitride, tungsten, tungsten nitride, or poly-silicon. In the preferred embodiment, the sacrificial layer SL 18x can be SiO₂ deposited by plasma enhanced chemical vapor deposition (PECVD), and the height or thickness of sacrificial layer 18x is preferably between 300 to 5000 Angstroms to provide a sufficiently large process window.

5 Referring to FIG. 3B, a photoresist is coated, exposed and then developed into an interconnect wiring pattern 22x. In FIG. 3C, the sacrificial layer 18x and metal layer 10x are formed into the same configuration as the interconnect wiring pattern 22x by an etch process, such as a plasma etch. As shown in FIG. 3D, photoresist stripping and wet clean steps are performed to leave metal or interconnect lines 10x with a sacrificial cap
10 layer 18x.

Referring to FIG. 3E, a low-k material 26x is deposited on the substrate 14x, metal lines 10x, and sacrificial layer 18x by chemical vapor deposition (CVD), or by spin-on coating followed by curing. The low-k material 26x can be made from a material which is chemically different from the material of the sacrificial layer 18x, and preferably has a
15 dielectric constant of less than four. In the preferred embodiment, the height or thickness of low-k material 26x is preferably between 3000 Angstroms to 20,000 Angstroms.

Non-limiting examples of the low-k material 26x include doped or non-doped SiO₂, polyimides, silsesquioxanes, fluorinated-polyimides, parylene, fluoro-polymers, poly(arylethers), fluorinated-poly(arylethers), porous-polymer/polyimide,
20 polytetrafluoroethylene, and porous silica (also known as Aerogel and Xerogel).

In addition, those skilled in the art will appreciate that if thick low-k films 26x are to be provided, multiple coatings and curing of the low-k film 26x may be needed if the low-k material 26x is to be deposited by a spin-on coating process.

Referring to FIG. 3F, low-k material 26x is removed by an etch-back process step
25 that leaves the low-k surface level somewhere within the height of the patterned sacrificial layer 18x (i.e., at a height that is greater than or equal to the height of the metal line and less than or equal to the height of the metal lines plus the height of sacrificial layer 18x) in the closely-spaced metal lines. The low-k etch-back can be accomplished by conventional methods. For example, a plasma etch having an etch rate of low-k material

26x that is faster than the etch rate of sacrificial layer 18x can be utilized. In a preferred embodiment, the low-k material is organic material and it can be etched by oxygen-based plasma.

5 The present invention employs the sacrificial layer 18x to allow both the closely spaced apart metal lines and the further spaced metal lines to meet the low-k material process window. The low-k material 26x has different heights or levels depending on the distance between the metal lines or the metal line density. For example, the level of the low-k material 26x is higher at the region of the metal lines 10x which are closely spaced, and the level of the low-k material 26 is lower at the region of the metal lines 10x which
10 are less closely spaced, and the level of the low-k material 26x is even lower at the region between the metal lines 10x which are spaced-apart from each other by a much larger spacing. Thus, the sacrificial layer 18x atop the metal lines 10x increases the process window. Alternatively, as described below, instead of a low-k etch-back, a CMP process can be used to polish back the low-k material 26x.

15 Referring to FIG. 3G, the sacrificial layer 18x is removed by employing an etch-back (e.g., a carbon-fluorine-based plasma etch if layer 18x is silicon dioxide). This etch is selective in that the etch chemistry removes the sacrificial layer 18x without attacking the dielectric layer 26x and metal lines 10x. Referring to FIG. 3H, a protective layer 20x is deposited on the low-k material 26x and the metal lines 10x. The protective layer 20x can
20 be a dielectric material such as a silicon nitride layer or a silicon carbon layer. Preferably, protective layer 20x is chemically different than dielectric layer 24x, which is deposited hereinafter. In the preferred embodiment, the height or thickness of protective layer 20x is preferably between 50 Angstroms to 1000 Angstroms. Referring to FIG. 3I, a conventional dielectric layer 24x, such as a SiO₂ layer, is deposited and planarized.
25 Dielectric layer 24x can also include silicon carbon (SiC), aluminum oxide (Al₂O₃), or other insulators which are preferably chemically different from protective layer 20x.

It is important that there is good etch selectivity between protective layer 20x and second insulator layer 24x. In the preferred embodiment, the height or thickness of

dielectric layer 24x after the planarization (e.g. by CMP) is preferably between 3000 Angstroms to 20,000 Angstroms above the metal lines 10x.

Referring to FIG. 3J, a via pattern is transferred to the wafer by conventional photolithography and plasma etch. An etch chemistry is utilized to etch vias through dielectric layer 24x. The etch stops at protective layer 20x. With protective layer 20x in place to protect low-k material 26x, conventional processing steps, such as photo-resist strip and post-via etch clean using solvents, can be performed. Protective layer 20x protects low-k material 26x from the chemicals utilized in the etch strip and wet clean process steps. Once all desired processing for the vias has been completed, a soft etch is performed to selectively remove protective layer 20x inside the via holes as is described in greater detail hereinafter with reference to FIGS. 3K, 3L, 7A and 7B.

In one embodiment, referring to FIG. 3K, after vias have been etched through dielectric layer 24x and cleaned, both horizontal portions and vertical portions of protective layer 20x inside the via holes are removed by an isotropic etch. It is desirable that the etch chemistry utilized to remove protective layer 20x provides good etch selectivity between protective layer 20x and metal lines 10x, between protective layer 20x and low-k material 26x (i.e., the etch chemistry attacks protective layer 20x at a much faster rate than it attacks metal lines 10x and low-k material 26x), and between protective layer 20x and dielectric layer 24x.

As can be seen in FIG. 7A, when an isotropic etch is utilized, all horizontal portions and vertical portions of protective layer 20x are removed so that a liner 70 can contact the top surface of metal lines 10x, the vertical (i.e., sidewall) portion of low-k material 26x, and a horizontal (i.e., the top horizontal surface 19x of the low-k material 26x) portion of low-k material 26x. When vias 38x are filled with conductive plugs, the plugs can contact the metal lines 10x. Metal plugs are formed by a conductive material (e.g., tungsten, copper or aluminum). The liner 70 is a precursor for plug metal deposition. An isotropic etch can be utilized if the liner 70 is deposited by a CVD technique which provides better sidewall and horizontal coverage.

In an alternative embodiment, referring to FIG. 3L, after the vias 38x have been etched through dielectric layer 24x and cleaned, only the horizontal portions (also referred to as bottom coverage) of protective layer 20x inside the via holes are selectively removed by an an-isotropic etch. As can be seen in FIGS. 3L and 7B, when an an-isotropic etch is utilized, only the horizontal portions of protective layer 20x inside the via holes are removed, and a spacer 40x remains. For example, a silicon nitride (SiN) spacer can be left on the vertical portions of the exposed low-k material 26x. After the etch of protective layer 20x, liner 70, 70B (commonly known also as a "seed", "adhesion", or "barrier" layer) is deposited in the vias to prepare for the deposition of plug metal in the vias. When compared with FIG. 7A, the presence of the vertical spacer section 40x decreases the cross-sectional area of contact plug and increases the via resistance. Liner 70, 70B (shown in FIGS. 7A and 7B) can include titanium, titanium nitride, tantalum, tantalum nitride, aluminum, copper, tungsten nitride, or a combination thereof in a stack structure.

For improved step coverage, liner 70 can be deposited by collimated, ionized metal plasma (IMP) or hollow cathode magnetron (HCM) sputtering deposition. Although the bottom coverage can be significantly improved, the sidewall coverage improvement is still limited for these techniques for features having a high aspect ratio as shown in FIG. 7A. Preferably, a spacer 40x is left in the vias. Leaving a spacer 40x improves the sidewall coverage of liner 70 because of the shape of the spacer. Improving the sidewall coverage (1) improves the metal growth and deposition of the metal plug, which leads to lower resistance; and (2) improves the isolation between the low-k material 26x and the plug metal 42x as shown in FIG. 7B. Isolation of the plug metal 42x from low-k material 26x can be important if the low-k material 26x is corrosive to the metal utilized for plug 42x. Even if the low-k material 26x is not corrosive to the metal utilized for plug 42x, certain metals, such as copper, can diffuse into the low-k material 26x, which is an undesirable result, if sidewall coverage is poor.

FIG. 3M illustrates the interconnect structure after metal plugs 42x are formed in the via holes 38x inside the insulator layer 24x according to techniques described

hereinabove, and a second metal wiring layer 46x is fabricated, again according to methods known in the art. Plug 42x and second metal layer 46x can be deposited in two separate process steps (i.e., tungsten deposition for forming the plug 42x followed by alloy deposition for the metal layer 46x) or as a single process step (i.e., depositing 5 aluminum or other alloy to fill the via 38x and to form the metal layer 46x at the same time).

Thus, the above-described poisoned via problems can be avoided by the provision and subsequent removal of a sacrificial layer 18x and a portion of protective layer 20x.

For misaligned vias, protective layer 20x isolates low-k material 26x from process 10 chemicals that can cause poisoned vias. The protective layer 20x protects the low-k material 26x from chemicals and other process elements used in the via etch, photoresist strip, and via wet clean processing steps. Spacer 40x improves liner sidewall coverage for better plug metal growth and deposition. Furthermore, spacer 40x improves isolation of low-k material 26x and plug metal 42x for better reliability.

FIRST EMBODIMENT: PROCESS UTILIZING A LOW-K ETCH-BACK STEP (PERFECTLY ALIGNED VIAS)

FIGS. 4A-4E are vertical cross-sectional views that illustrate selected stages of fabrication of the interconnect structure according to the first embodiment of the present invention where perfect alignment between via and metal line can be obtained. Referring 20 to FIG. 4A, a substrate 14p is provided. Substrate 14p may, for example, include transistors, diodes, and other integrated circuit elements (not shown). A first metal layer 10p is deposited over substrate 14p. Metal layer 10p can include electrically conducting material, such as aluminum, titanium, or titanium-nitride, although other conductive 25 material can be employed. Sacrificial layer 18p is deposited on first metal layer 10p. Sacrificial layer 18p includes a height that is used to increase the process window for low-k material 26p etch-back as described previously.

First metal layer 10p and sacrificial layer 18p are patterned to form metal lines each having a sacrificial layer cap. Thereafter, a low-k material 26p is deposited to fill the gaps between the metal lines.

Referring to FIG. 4B, low-k material 26p is removed by an etch-back process step.

5 Low-k material 26p is etched-back to a height within the height of sacrificial layer 18p (i.e., at a height that is greater than or equal to the height of the metal line 10p and less than or equal to the combined height of the metal line 10p and the sacrificial layer). The sacrificial layer 18p is removed by employing an etch-back (e.g., a carbon-fluorine-based plasma etch if layer 18p is silicon dioxide). This etch is selective in that the etch
10 chemistry removes the sacrificial layer 18p without attacking the dielectric layer 26p and metal lines 10p. Referring to FIG. 4C, a protective layer 20p is deposited to cover the metal lines 10p and the low-k material 26p. An insulative layer (e.g., a dielectric) 24p is also deposited over protective layer 20p and planarized by a CMP process step.

Referring to FIG. 4D, vias 38p are etched into insulative layer 24p. In this case,
15 the vias 38p are perfectly aligned with the metal lines. A clean step is then performed for the vias 38p. An opening is formed in protective layer 20p using the techniques described above so that a metal, which is deposited in the vias 38p in a subsequent process step, can contact the first metal layer 10p. Liners can also be provided in the vias 38p. Referring to FIG. 4E, vias 38p are filled with metal plugs 42p. Thereafter, a
20 second metal layer 46p is deposited and patterned on insulative layer 24p.

SECOND EMBODIMENT: PROCESS UTILIZING LOW-K POLISH STEP INSTEAD OF LOW-K ETCH-BACK STEP

FIGS. 5A-5H are vertical cross-sectional views that illustrate selected stages of
25 fabrication of the interconnect structure according to a second embodiment of the present invention. FIG. 5A is a vertical cross-sectional view of the interconnect structure after the processing steps illustrated in FIGS. 3A-3E (i.e., after metal layer 10y and sacrificial layer 18y have been deposited on substrate 14y and patterned, and low-k material 26y has been deposited to fill gaps between metal lines 10y and to cover sacrificial layer 18y).

Referring back to FIG. 5B, low-k material 26y is removed by a chemical mechanical polish (CMP) process step.

For the sake of brevity, since FIGS. 5C-5I correspond generally to FIGS. 3G-3M, the description of FIGS. 3G-3M, 7A, and 7B as they relate to FIGS. 5C-5I will not be repeated herein. Instead, it is noted that the interconnect structure differs from that of the second embodiment in the following ways: (1) low-k material 26y is polished instead of etched-back; and (2) because of the planarization caused by the CMP, low-k material 26y has a height that is about the same in both the areas having the closely-spaced metal lines 10y and the areas having lines 10y that are spaced further apart.

THIRD EMBODIMENT: PROCESS UTILIZING BOTH A LOW-K PLANARIZATION STEP AND A LOW-K ETCH-BACK STEP

FIGS. 6A-6D are vertical cross-sectional views that illustrate selected stages of fabrication of the interconnect structure according to a third embodiment of the present invention. FIG. 6A is a vertical cross-sectional view of the interconnect structure after the processing steps illustrated in FIGS. 3A-3E, (i.e., after metal layer 10z and sacrificial layer 18z have been deposited on substrate 14z and patterned, and low-k material 26z has been deposited to cover substrate 14z and gap fill metal layer 10z and sacrificial layer 18z). Referring to FIG. 6B, low-k material 26z is removed by a CMP process step to a level that is higher than the sacrificial layer 18z. Referring to FIG. 6C, low-k material 26z is further removed by an etch-back process, such as by plasma etch. Referring to FIG. 6D, sacrificial layer 18z is then removed.

The processing steps in this embodiment that occur after FIG. 6D correspond generally to FIGS. 3H-3M and FIGS. 5D-5I previously illustrated and described for the first and second embodiments, respectively. For the sake of brevity, these previously described structures and process steps will not be described further herein. It is noted that the interconnect structure of this embodiment is structurally the same as the second embodiment, and reference is made to FIGS. 5D-5H, 7A and 7B. The difference between the second and third embodiments is in the extra process step of etch-back after

the chemical mechanical polish (CMP) step. The present embodiment is especially suited for the scenario where polishing organic low-k materials is difficult to accomplish, since the etch-back step following the initial polishing step will remove the surface defects generated in the low-k material polishing step.

5 Although the structure and processes of the present invention have been described in connection with one metal interconnect layer, the processes described herein can be used in the formation of a plurality of metal interconnect layers.

The present invention provides robust and manufacturable low-k dielectric interconnect processes and corresponding structures. A sacrificial layer, embodying the
10 metal pattern, is fabricated on top of the metal before the low-k dielectric is deposited onto the wafer. The sacrificial layer increases the final thickness of the low-k material after the low-k dielectric etch-back or CMP. An increase in the low-k material between the metal gaps leads to lower inter-line capacitance, improving performance of the circuits.

Furthermore, the processes of the present invention do not require an additional
15 mask/lithography step, and as discussed previously, increases the process window for the low-k dielectric process. The protective layer isolates the low-k material from the chemicals that are employed to etch and clean the vias so that poisoned via problems can be avoided. The spacer can improve liner step coverage for better plug metal fill and improve isolation between the low-k material from the metal plug in certain scenarios
20 thereby improving process robustness and reliability of the interconnect.

It will be recognized that the above described invention may be embodied in other specific forms without departing from the spirit or essential characteristics of the disclosure. Thus, it is understood that the invention is not to be limited by the foregoing illustrative details, but rather is to be defined by the appended claims.

What is claimed is:

1. A method for forming an interconnect structure on a semiconductor body, comprising the steps of:

- (a) depositing a first metal layer on a semiconductor body;
- 5 (b) depositing a sacrificial layer on the first metal layer, said sacrificial layer having a height;
- (c) patterning the sacrificial layer and the metal layer to form separate metal lines with a sacrificial layer cap on said metal lines;
- 10 (d) depositing a low-k material to fill gaps between metal lines and to cover the sacrificial layer;
- (e) removing the low-k material to a level within the height of the sacrificial layer;
- (f) removing the sacrificial layer; and
- 15 (g) depositing a protective layer to cover the metal lines and the low-k material.

2. The method of claim 1, wherein the step of removing the low-k material to a level within the height of the sacrificial layer includes the step of etching back the low-k material to a level within the height of the sacrificial layer.

20 3. The method of claim 2 wherein step of etching back the low-k material to a level within the height of the sacrificial layer includes a plasma etch step.

25 4. The method of claim 1, wherein the step of removing the low-k material to a level within the height of the sacrificial layer includes the step of polishing the low-k material to a level within the height of the sacrificial layer.

5. The method of claim 4, wherein the step of polishing the low-k material to a level within the height of the sacrificial layer includes a chemical mechanical polish (CMP) step.

6. The method of claim 1, wherein the step of removing the low-k material to a level within the height of the sacrificial layer includes the steps of polishing the low-k material and etching back the low-k material.

7. The method of claim 6, wherein the steps of polishing the low-k material and etching back the low-k material includes a plasma etch step and a chemical mechanical polish (CMP) step.

8. The method of claim 1, further comprising the steps of:
depositing an insulator on the protective layer;
creating vias in the insulator;
performing a photoresist strip; and
performing a set clean.

9. The method of claim 8, further comprising selectively etching the protective layer.

10. The method of claim 9, wherein selectively etching the protective layer further includes the step of utilizing an isotropic etch.

11. The method of claim 9, wherein selectively etching the protective layer further includes the step of utilizing an an-isotropic etch to leave a spacer on a vertical portion of the low-k material in the vias.

12. The method of claim 9, further comprising filling the vias with a metal.

13. The method of claim 12, further comprising depositing and patterning a second metal layer over the insulator.

14. The method of claim 13, wherein the sacrificial layer is made of a material selected from the group consisting of an oxide, silicon oxide, aluminum oxide, silicon nitride, silicon carbide, a polymer, an organic material, a conductive material, titanium,
5 titanium nitride, tungsten, tungsten nitride, and poly-silicon.

15. The method of claim 9, further comprising simultaneously depositing the plug metal and second metal layer at the same time, followed by patterning of the second metal layer.

10

16. An interconnect comprising:

(a) one or more metal lines formed from a first metal layer, said metal lines having gaps therebetween;

(b) low-k material filling the gaps between the metal lines and having a height
15 and one or more vertical portions;

(c) a protective layer formed over the metal lines and the low-k material, wherein the protective layer covers at least one vertical portion of the low-k material;

(d) a dielectric layer formed over the protective layer;

(e) one or more vias etched in the dielectric layer;

(f) a metal for filling the vias;
20

(g) a second metal layer formed over the dielectric layer; and

(h) one or more openings in the protective layer for allowing the metal in the vias to contact the first metal lines.

25 17. The interconnect of claim 16, wherein the protective layer includes an oxide.

18. The interconnect of claim 17, wherein the oxide includes silicon dioxide.

19. The interconnect of claim 16, wherein the protective layer includes a dielectric material.

20. The interconnect of claim 19, wherein the protective layer includes silicon
5 nitride.

21. The interconnect of claim 16, wherein the protective layer includes silicon carbon.

10 22. The interconnect of claim 16, further comprising a spacer disposed on the vertical portion of the low-k material in the vias.

23. The interconnect of claim 16, wherein the protective layer is silicon nitride.

15 24. The interconnect of claim 16, wherein the first metal layer is an aluminum alloy, the metal filling the vias is tungsten, and the second metal layer is an aluminum alloy.

20 25. The interconnect of claim 16, wherein the first metal layer is an aluminum alloy, the metal filling the vias is an aluminum alloy, and the second metal layer is an aluminum alloy.

26. The interconnect of claim 16, wherein the dielectric layer is made of silicon dioxide, the protective layer is silicon nitride, and the low-k material is an organic low-k
25 material.

27 The interconnect of claim 16, wherein the dielectric layer is made of silicon dioxide, the protective layer is silicon nitride, and the low-k material is a porous silicon dioxide.

ABSTRACT OF THE INVENTION

A method is provided for forming an improved interconnect structure on a semiconductor body. A first metal layer is deposited on the semiconductor body. A sacrificial layer having a height is deposited on the first metal layer. The sacrificial layer and the metal layer are patterned to form separate metal lines with the sacrificial layer remaining on said metal lines. A low-k material is then deposited to fill the gaps between metal lines and to cover the sacrificial layer. The low-k material is then removed to a level within the height of the sacrificial layer. The sacrificial layer is then removed. A protective layer is deposited on top of the metal lines and the low-k material. A dielectric layer is deposited over the protective layer. The protective layer protects the low-k material from attack by chemicals utilized by subsequent process steps to etch vias in the dielectric layer, to strip photo-resist, and to clean the vias. The protective layer is then selectively etched away to make contact between a via plug and the metal lines.

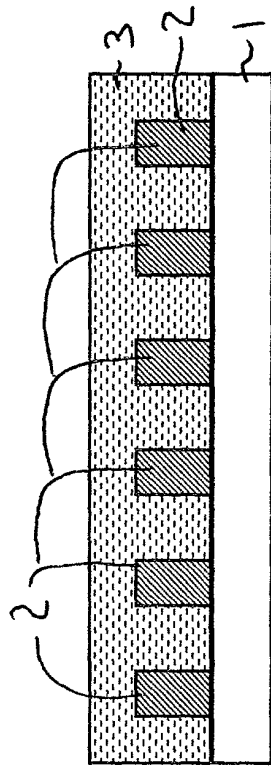


FIG. 1(A)

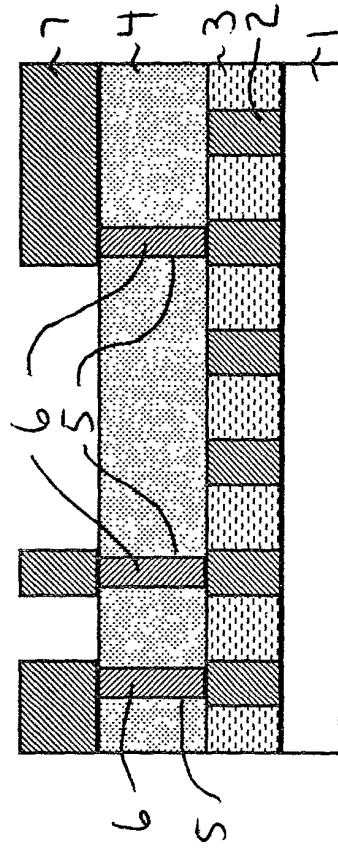


FIG. 1(B)

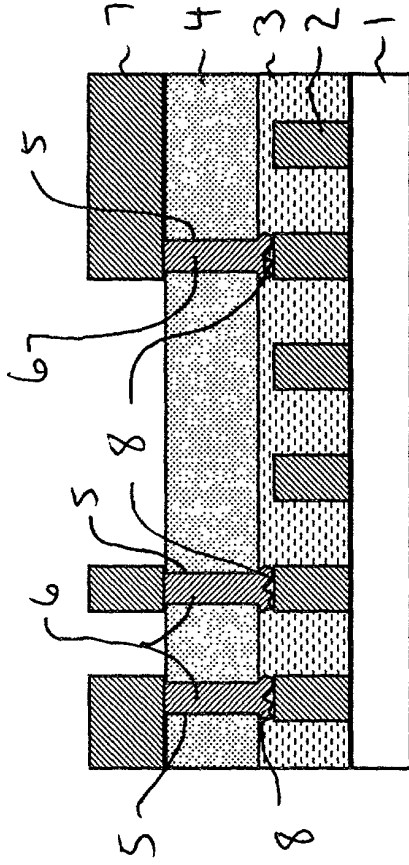


FIG. 1(C)

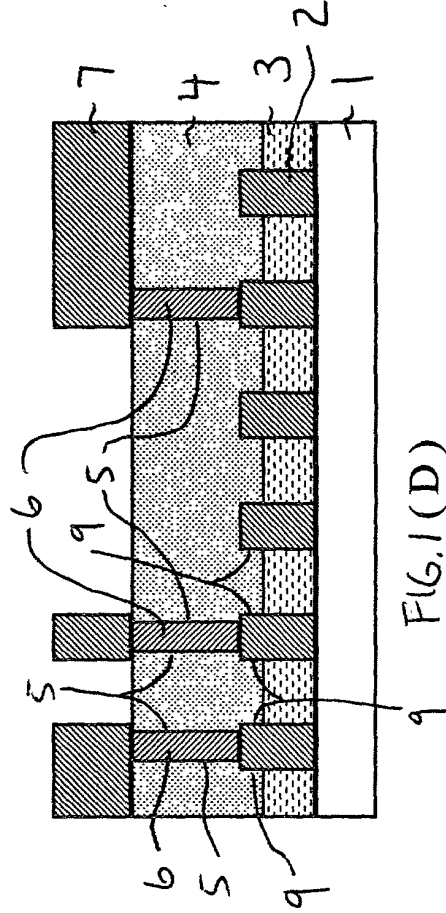


FIG. 1(D)

PRIOR ART

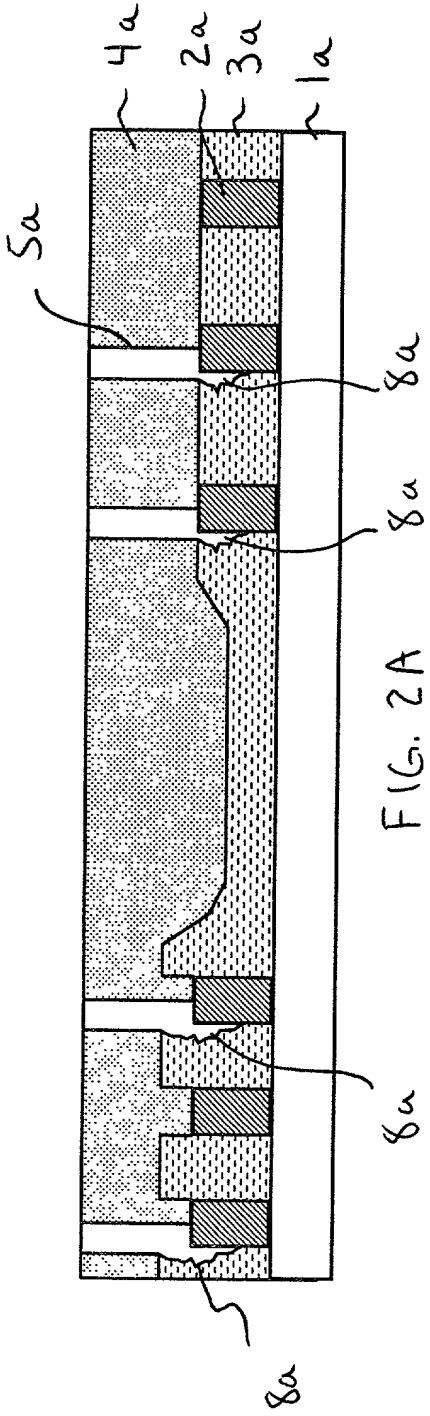


FIG. 2A

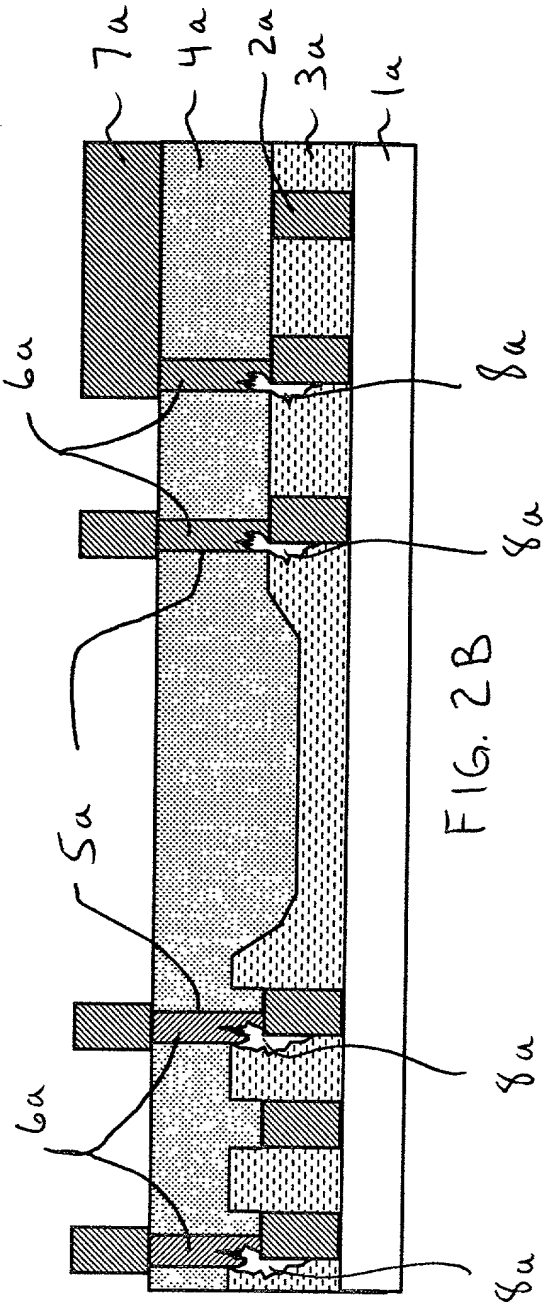


FIG. 2B

PRIOR ART

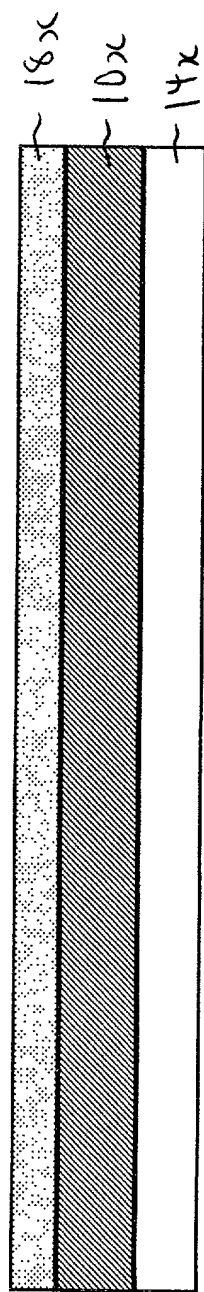


FIG. 3A

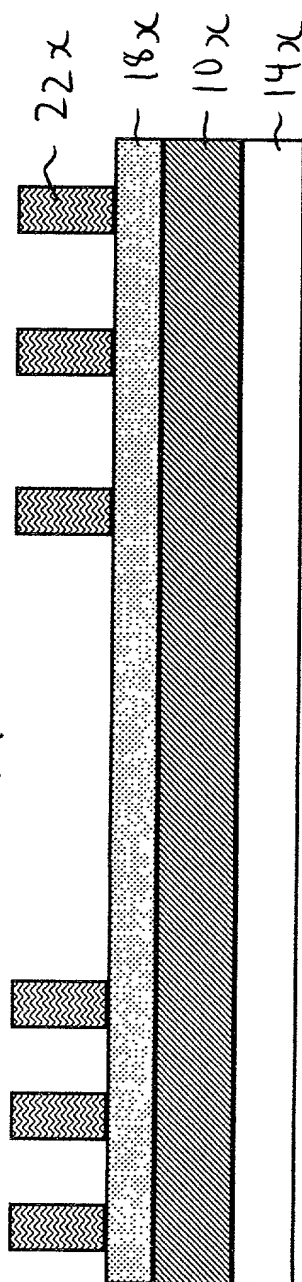


FIG. 3B

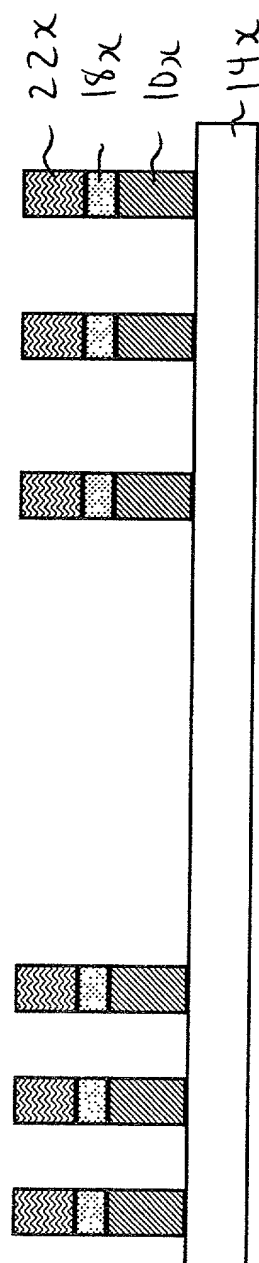


FIG. 3C

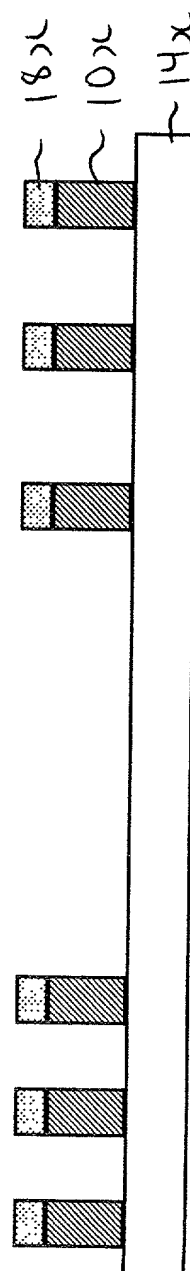


FIG. 3D

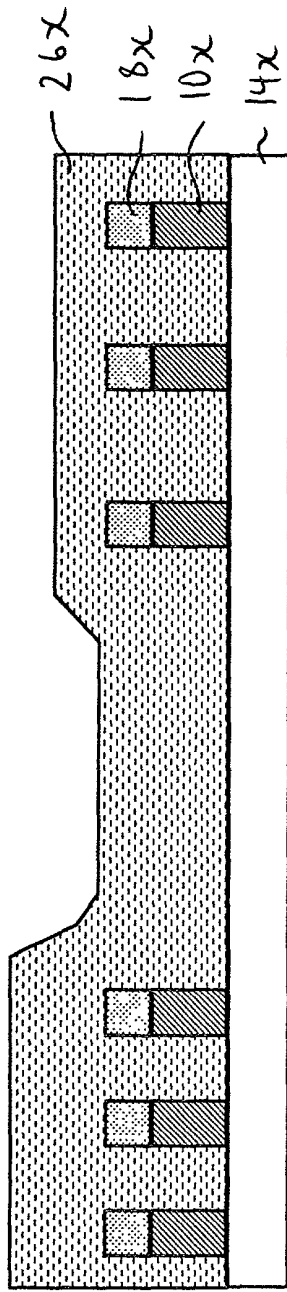


FIG. 3E

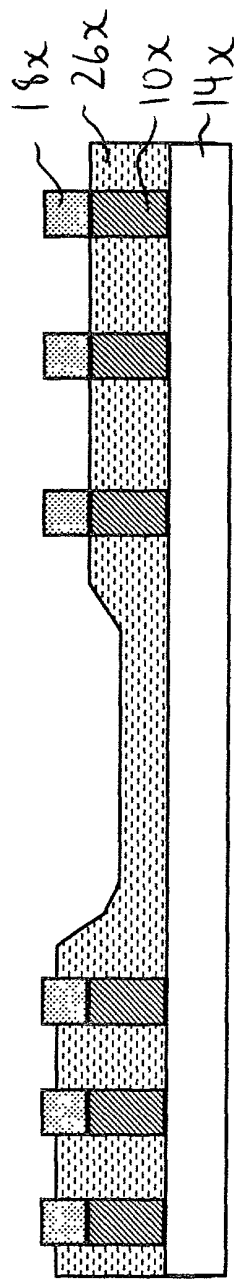


FIG. 3F

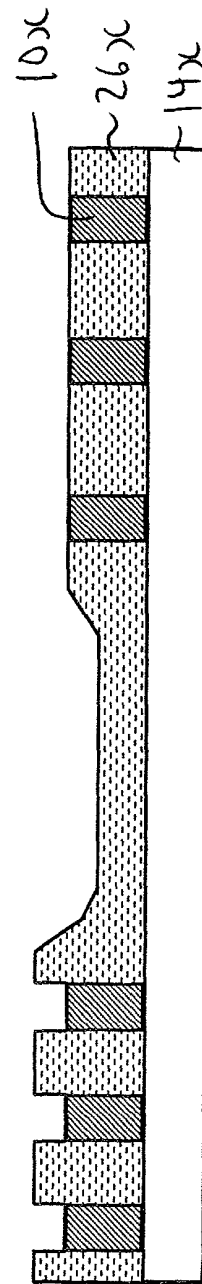


FIG. 3G

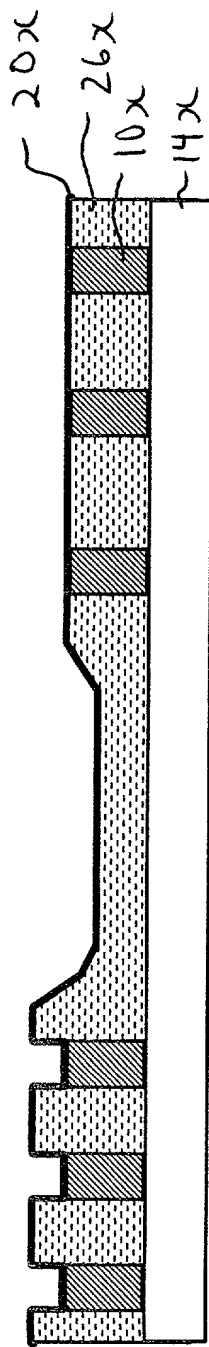


FIG. 3H

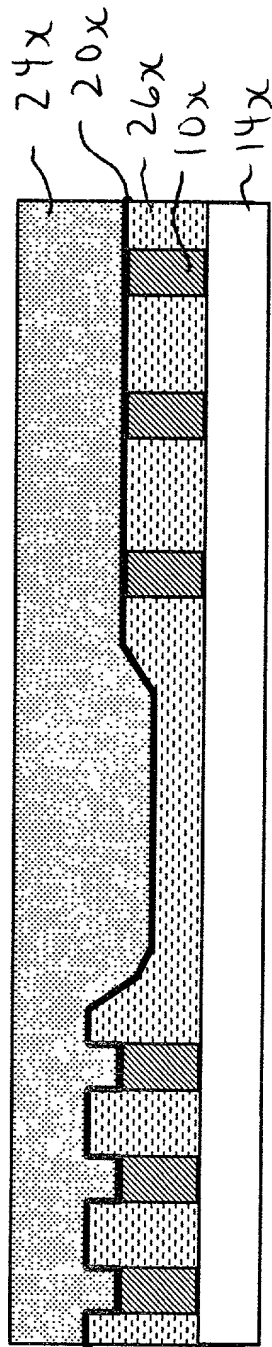


FIG. 3I

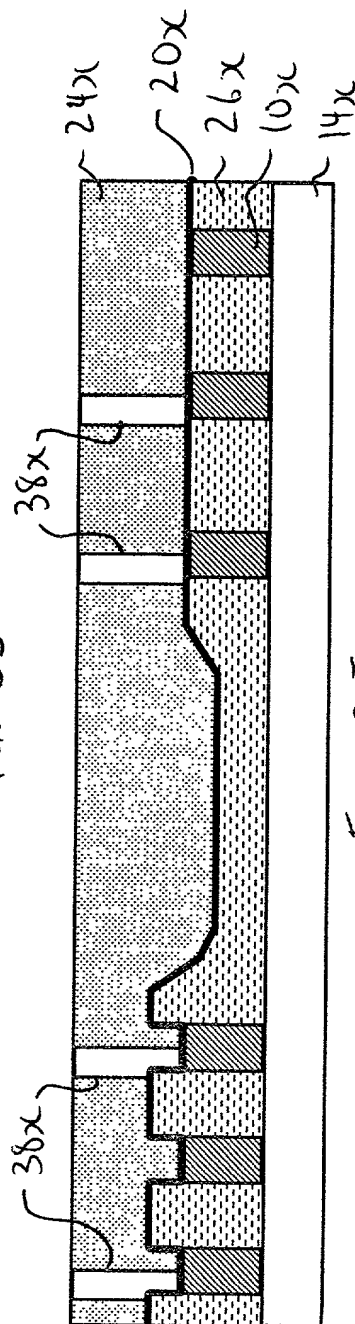


FIG. 3J

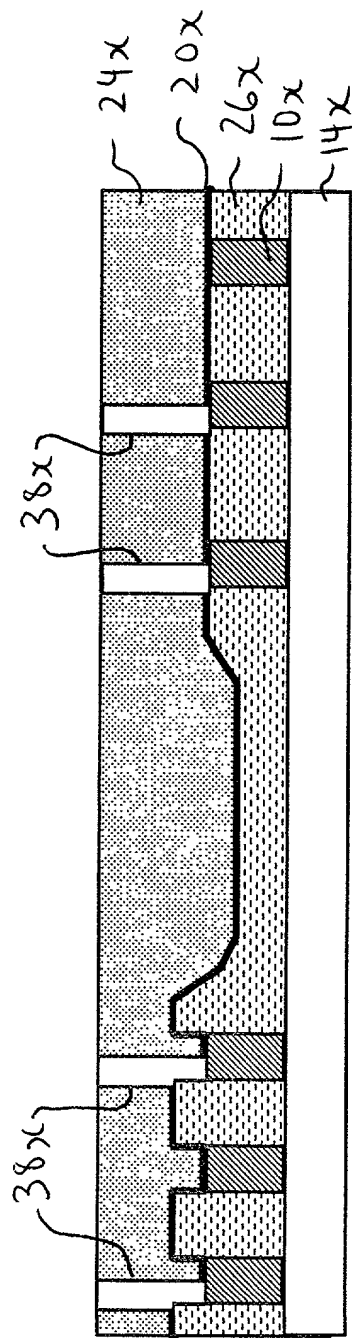


FIG. 3K

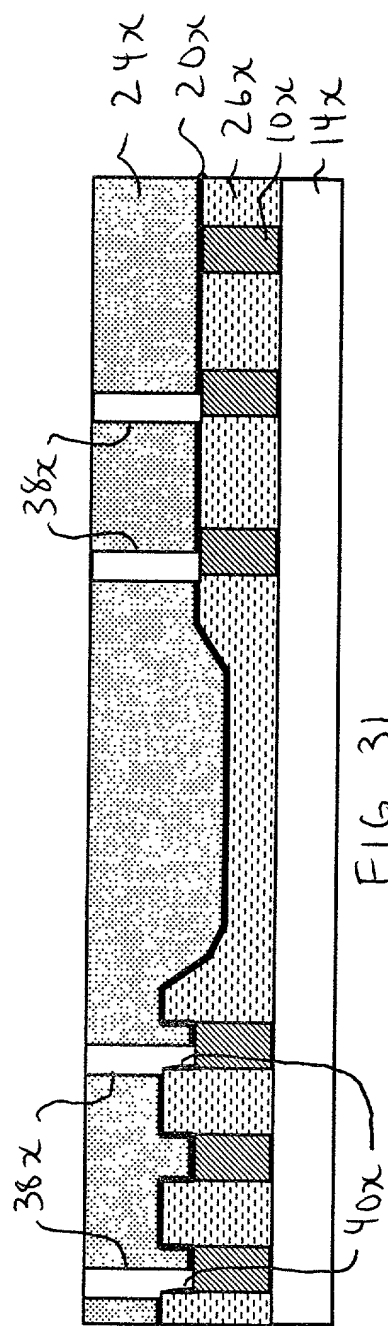


FIG. 3L

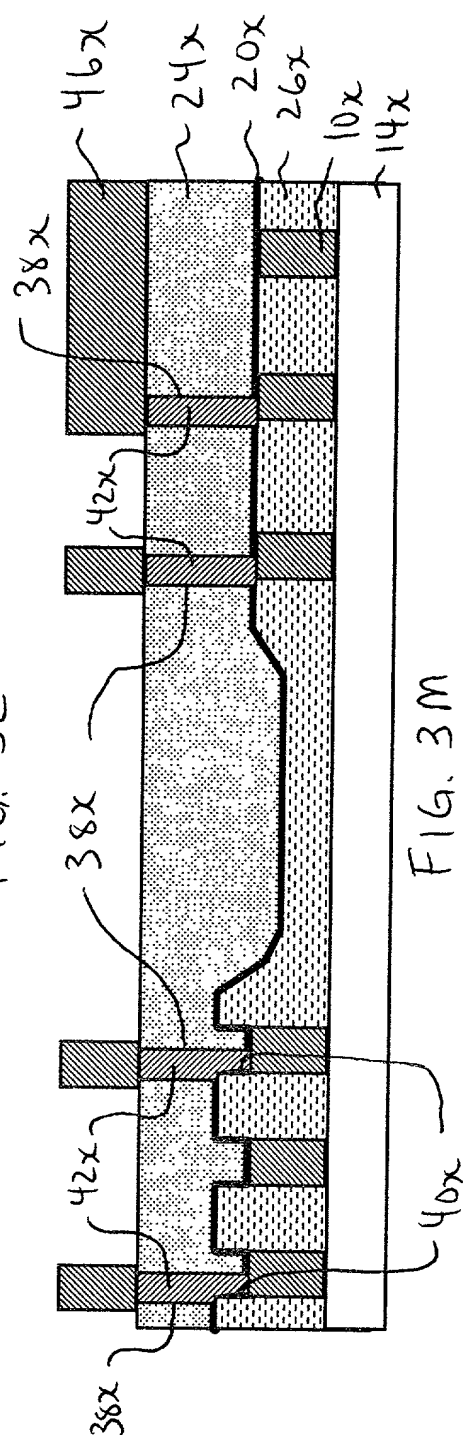


FIG. 3M

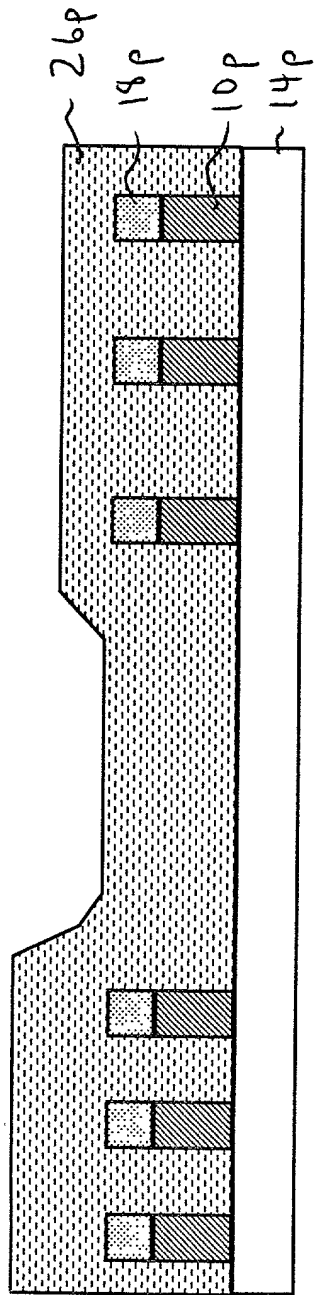


FIG. 4A

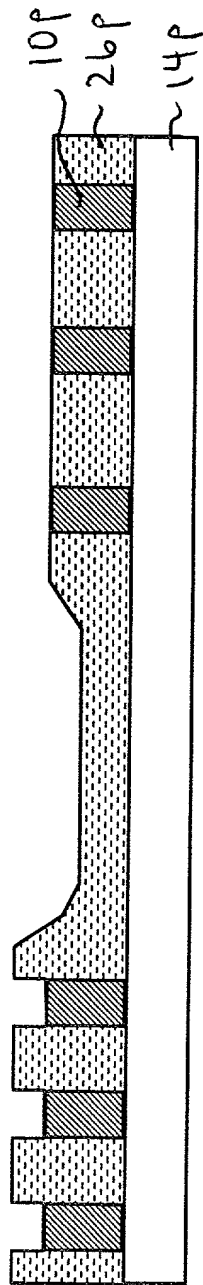


FIG. 4B

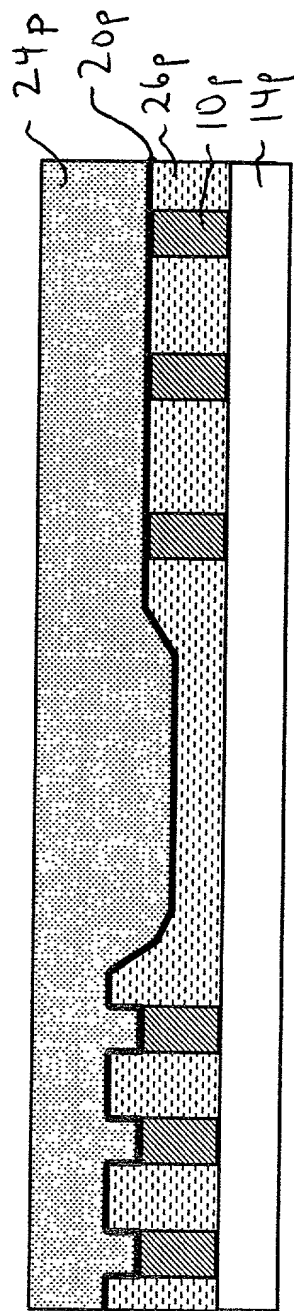


FIG. 4C

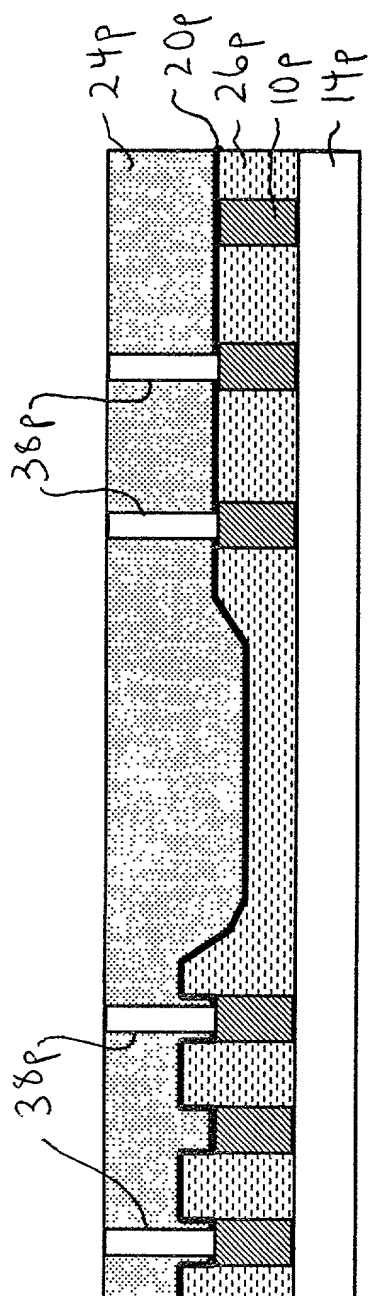


FIG. 4D

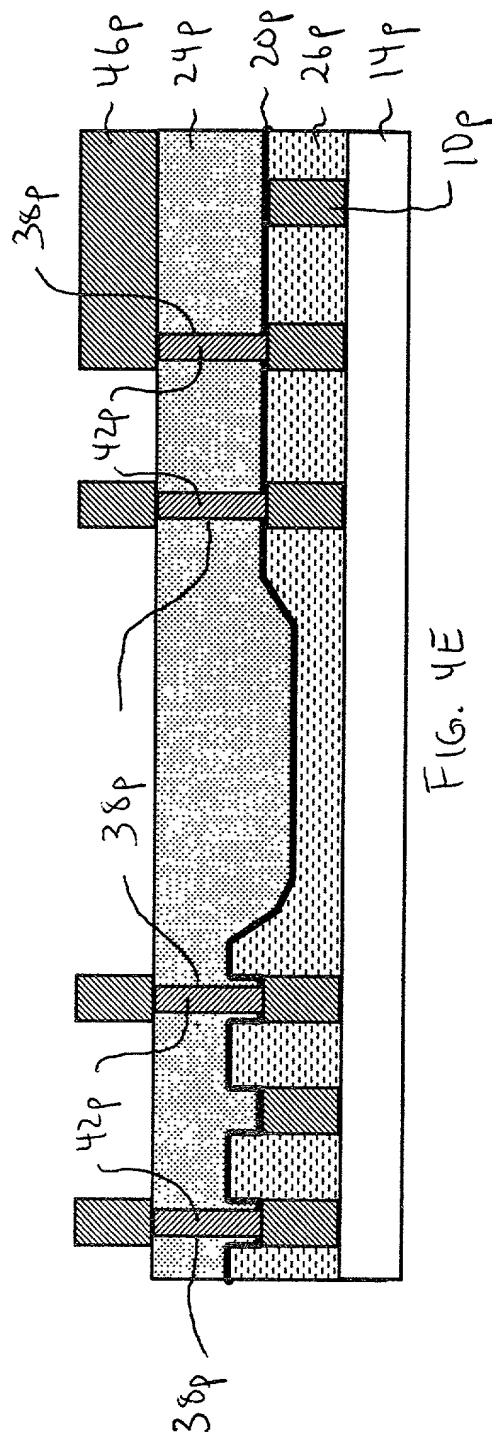


Fig. 4E

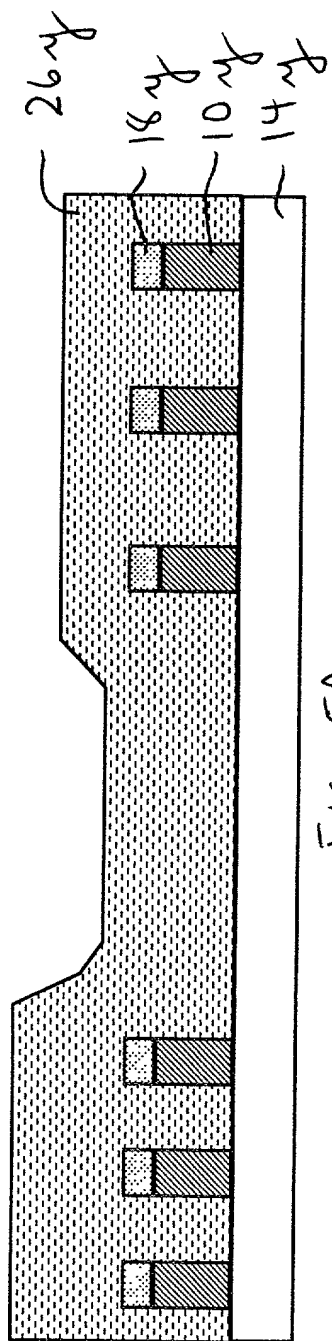


FIG. 10A

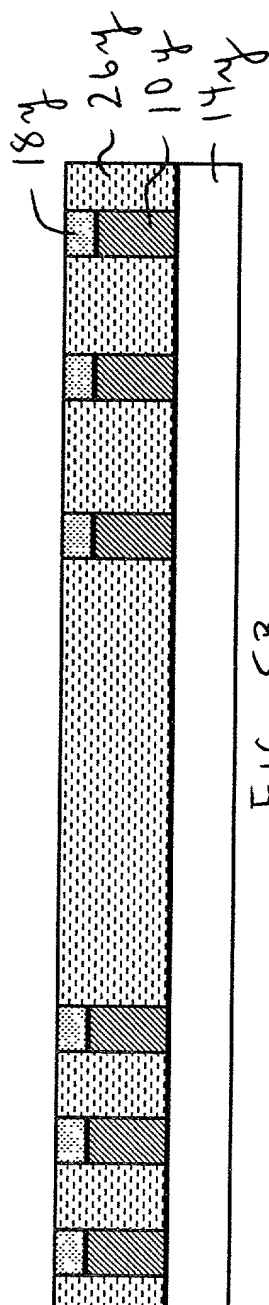


FIG. 10B

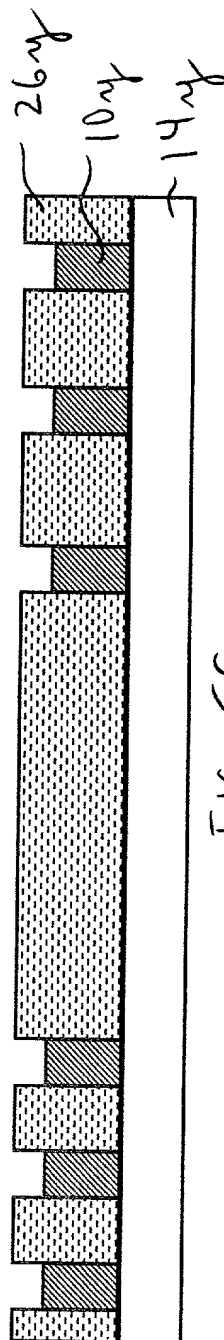


FIG. 10C

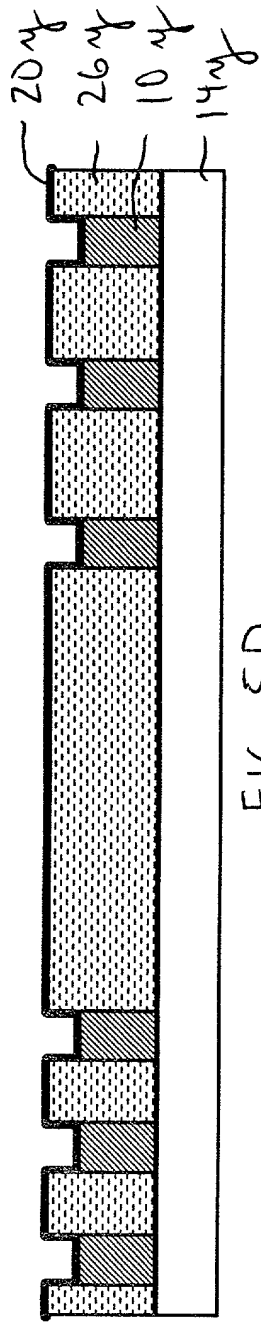


FIG. 5D

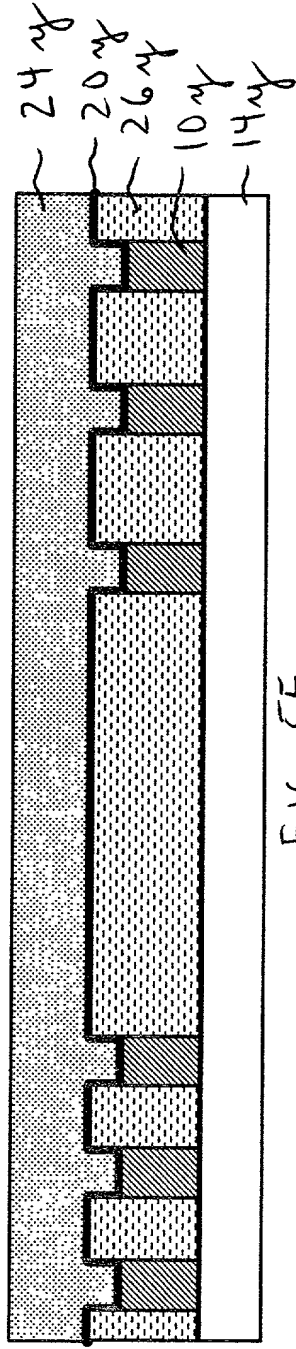


FIG. 5E

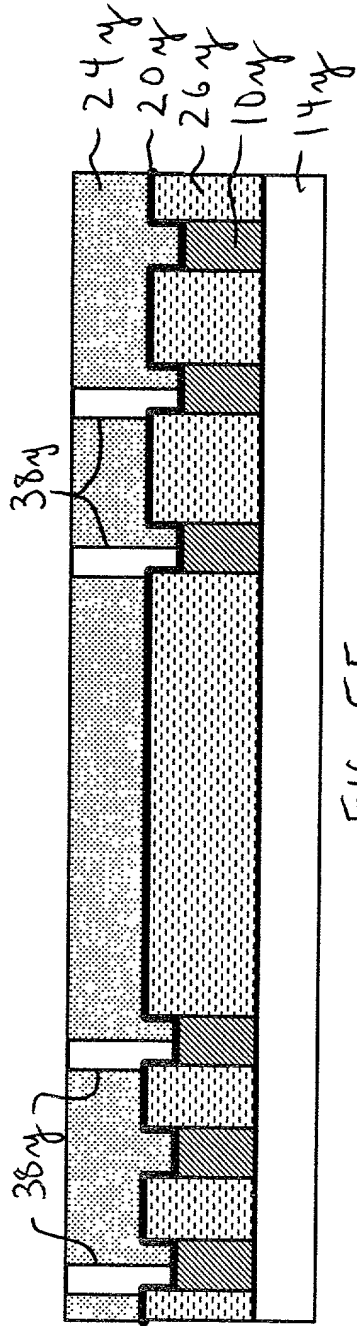


FIG. 5F

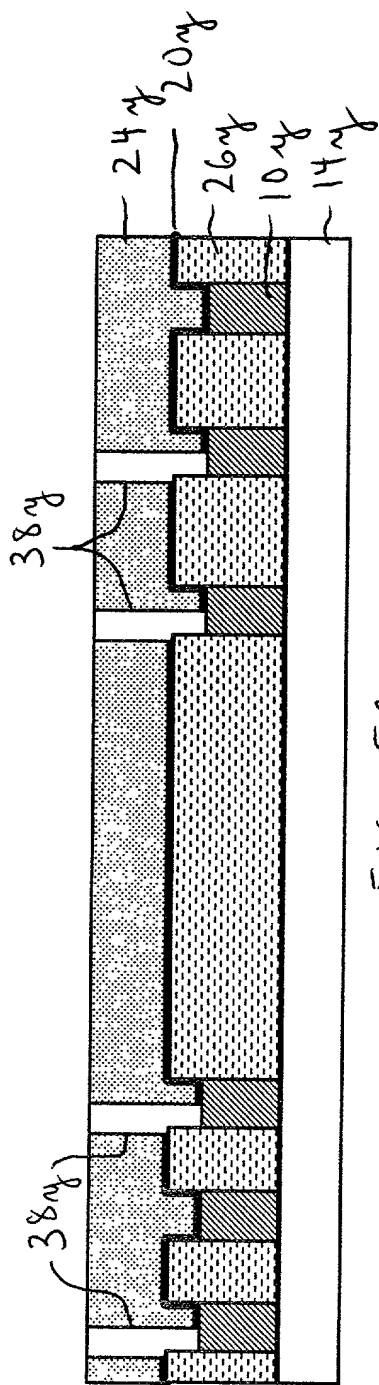
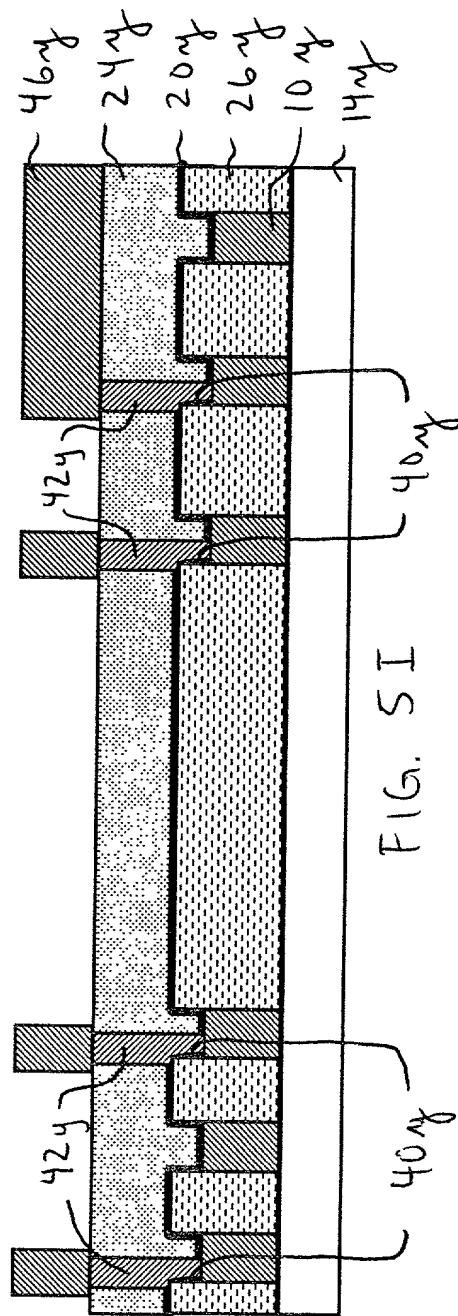
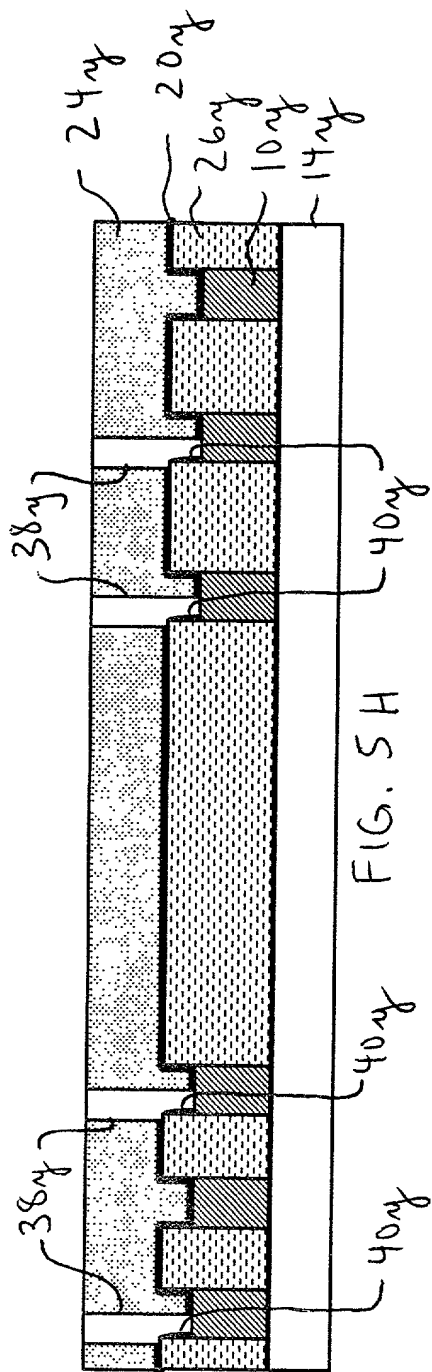


FIG. 5G



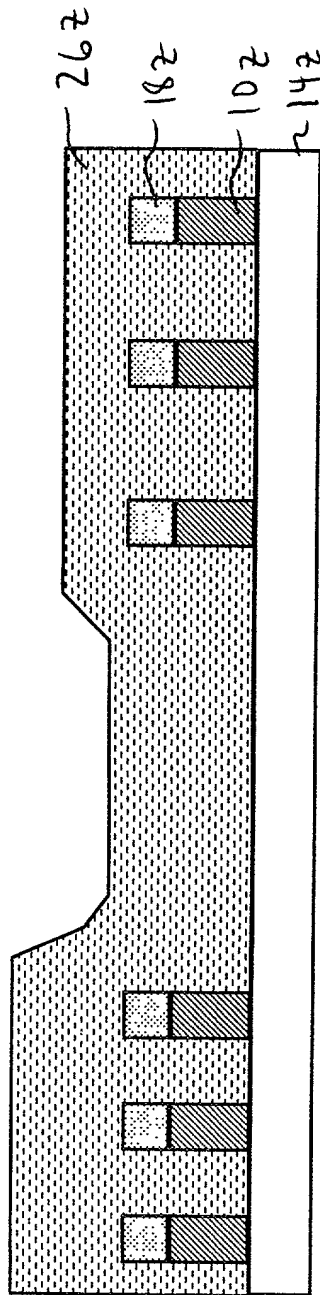


FIG. 6A

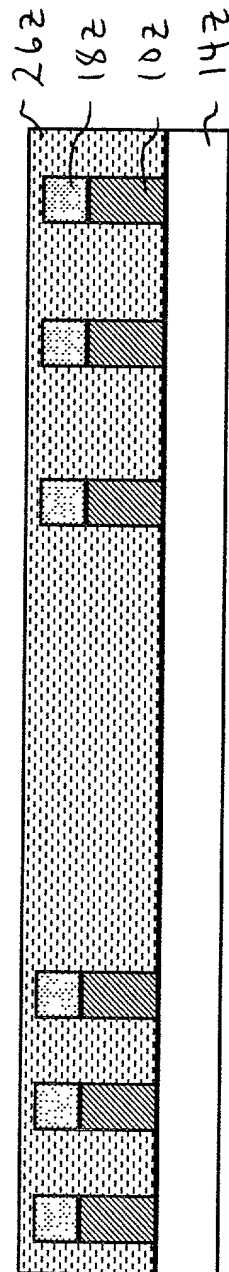


FIG. 6B

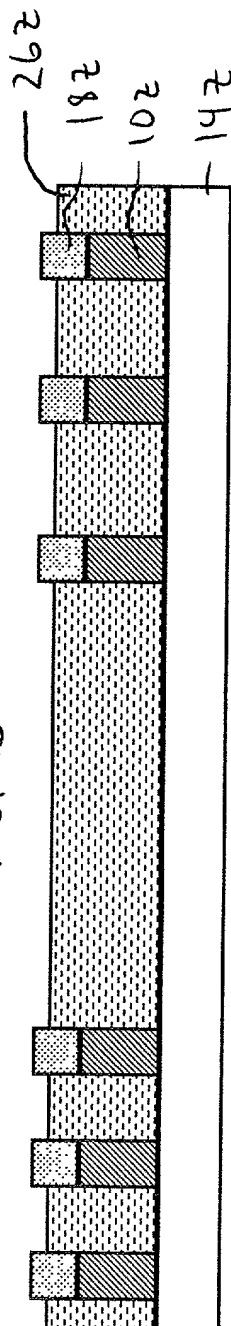


FIG. 6C

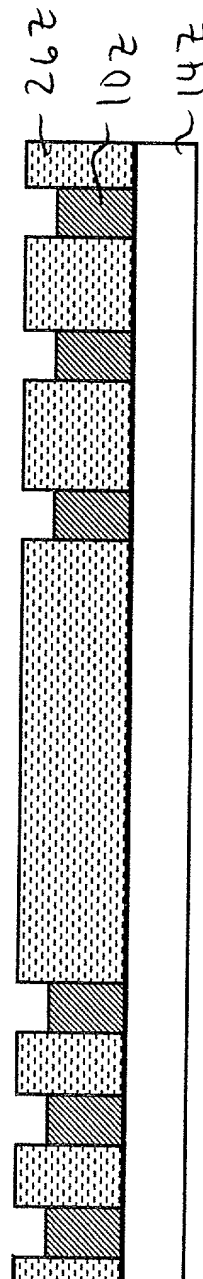
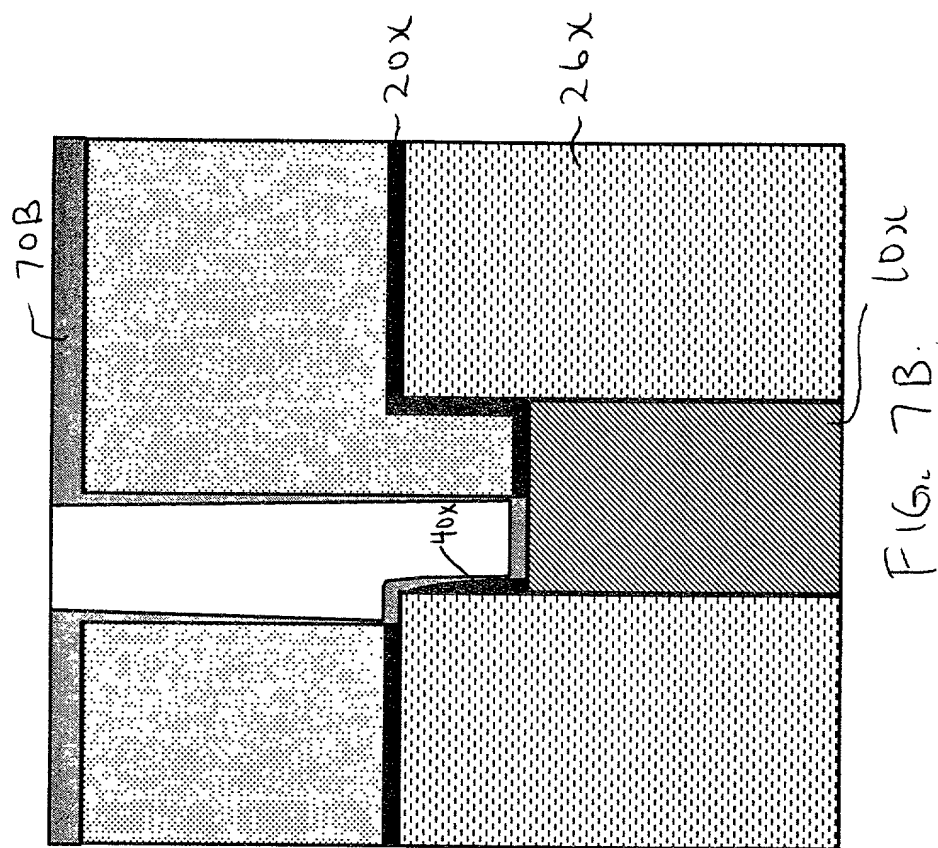
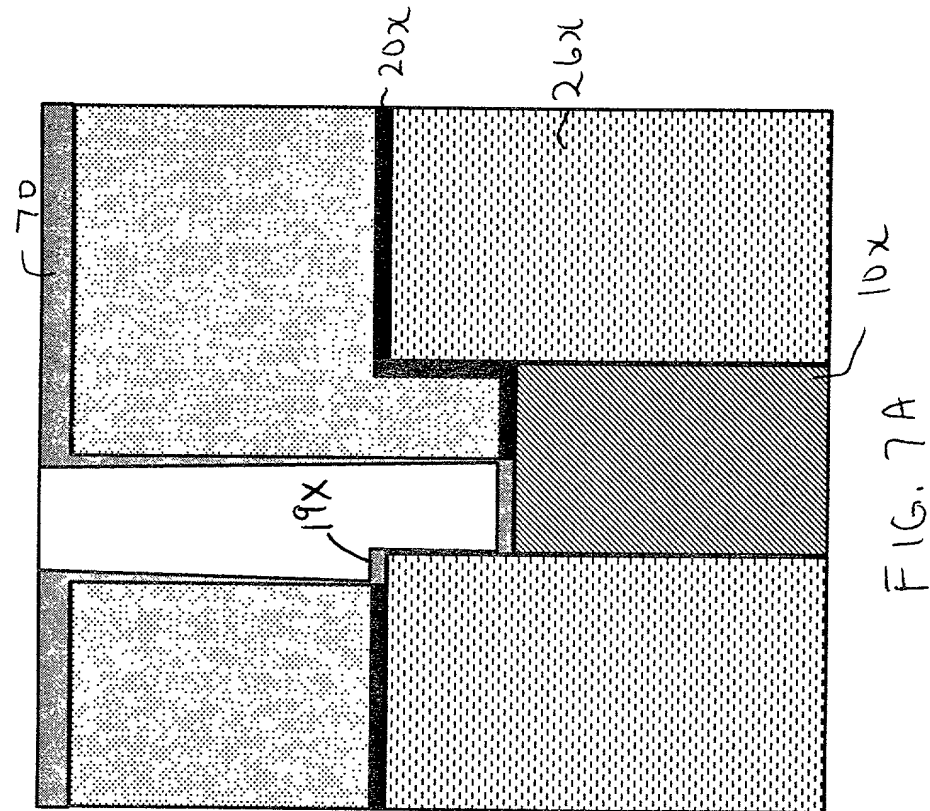


FIG. 6D



DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are stated below next to my name.

I believe that I am the original, first and sole (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled Interconnect with Low Dielectric Constant Insulators for Semiconductor Integrated Circuit Manufacturing, the specification of which is:

- (X) attached hereto, or
() was filed on _____
as Application Serial No. _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application are not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

Application Serial No. _____	Filing Date _____	Status _____
Application Serial No. _____	Filing Date _____	Status _____

I hereby appoint the following attorney(s) and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

William C. Cray, Reg. No. 27,627, Philip K. Yu, Reg. No. 35,742, Susie H. Oh, Reg. No. 36,391, Joseph W. King, Jr., Reg. No. 35,768, Raymond Sun, Reg. No. 35,699, and Eric Ho, Reg. No. 39,711, with full power of substitution and revocation hereby given to William C. Cray.

Address all telephone calls to Philip K. Yu at telephone no. (949) 221-3203

Address all correspondence to:

Rockwell Semiconductor Systems, Inc.
c/o Intellectual Property Department, Mail Code E09-900
4311 Jamboree Road
Newport Beach, CA 92660-3095

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of inventor 1: Bin Zhao

Inventor's signature: Bin Zhao Date: 9/11/98

Residence: Irvine, California

Citizenship: People's Republic of China

Post Office Address: 14 Figaro, Irvine, CA 92606

Full name of inventor 2: Maureen R. Brongo

Inventor's signature: Maureen R. Brongo Date: 9-11-98

Residence: Laguna Hills, California

Citizenship: U.S.

Post Office Address: 27381 Lost Trail Drive, Laguna Beach, CA 92653